European X-ray Free-Electron Laser Facility

- An ESFRI project, whose construction started in January 2009 in Hamburg, Germany.
- Intense, ultra short and coherent X-ray pulses will be used to investigate nm-scale structures, fast processes, and extreme states.
- From 2016 six experiment stations will operate at three of the five beam lines under construction.

Throughput and Processing at the European XFEL

Electronics Developments for High Speed Data Throughput and Processing at the European XFEL

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Pulse delivery time structure

- Pulses are delivered at 4.5 MHz for periods of 600 µs with a nominal 10 Hz pulse train repetition rate.
- The 10 Hz train delivery frequency is exploited in front- and backend DAQ and electronics to synchronize and pipeline data processing.

Electronics

- MTCA 4 and ATCA crates
- Xilinx FPGAs and IDEs
- Simulink development framework for user code
- Network f/w upgrades

DAQ and control Front End Interfaces

- 10 Gbps (SFP+) UDP or TCP – DAQ readout
- 0.1 or 1 Gbps (RJ45) TCP – Device control
- 3.125 Gbps (SFP) LLXP – Pulse VETO
- PCIe or serial lines – Sync, trigger, tagging

Timing interface

The double width AMC Timing Receiver board developed by the e-machine controls group is used to receive and distribute triggers, clocks and tagging information to photon beam line and experiment DAQ and control sub-systems.

Slow timing interface

Interfacing of slow 10-30Hz, remote, or non-MTCA hosted systems is made using the External Timing Adapter (ETA) board.
- ETA is driven by a Timing Receiver (TR)
- TR inputs provided over ETA’s RJ45 connector
- 3 configurable trigger, clock, or metadata CML lines
- 5V power line
- Application usage examples
- Image acquisition triggering (GigE)
- PLC synchronization
- Gotthard and delay line detectors
- Laser synchronization

2D detector trigger, clock, tag, and VETO synchronizer

A double width AMC synchronizer has been implemented for use with 2D detectors developed for the facility. The system consists of a DAMC2 front side digital board and a Rear Transition Module, interconnected by the MTCA.4 upper, non-backplane, 60pin ADF connector.
- The system is driven by a Timing Receiver (TR)
- TR inputs provided over the backplane
  - Using point-to-point and bussed lines
- Application usage examples
  - An uninterrupted stable 99 MHz clock
  - Train start, stop and reset trigger events
  - Metadata: train number, pulse pattern
  - Pulse frequency aligned VETO decision

Readout and Processing

Digitizer developments

Many detectors require analog-to-digital conversion at rates between 4.5MS/s and 10 GS/s. Collaborating with SP-Devices a MicroTCA double width AMC mother board has been developed onto which SP-Devices digitizers (PCIe form factor), as mezzanines, are mounted.

- Mother board comprising of:
  - MTCA 4 form factor
  - Single 10 Gbps (SFP+) data link
  - Single 3.125 Gbps (SFP) feedback link
  - SP-Devices mezzanine comprising of:
    - Virtex 6 FPGA for data processing and result/data transfer to backend interfaces
    - Digitizer types: SDR14, ADQ108, ADQ412, ADQ1600, ADQDSP

Pulse trigger system

A VETO trigger is being developed to reject poor quality images during the 600 µs delivery envelope.

- Implemented using LLP messaging on SFP interface
- Custom Low Level Protocol minimizes FPGA-FPGA delay
- Input information provided by fast detectors (APD, eTOF. . . )
- Keep/Reject decision clause evaluation in control FPGA
- Output to front and electronic interfaces