Timing System Developments Based on White Rabbit

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Requirements
- Clock, events and timestamp distribution
- Upper-bound latency of event distribution
- Timing events 1ns resolution
- Machine Cycle from 20ms up to hours
- 2000 Front End Controllers (FEC)
- True parallel operation
- Reliable and robust

Design
- Timing Master
  Timing is distributed in the network from a WR switch configured as master. The master uses the 10 Mhz and PPS signal from a GPS for synchronization and the UTC Time for the synchronization of the network.

Timing Network
- WR switches
- Timing and Data resilience against network failures is achieved using redundant connections. Upper-bound delivery latency guaranteed using a QoS and Cut-through switching.

Data Master
- Take machine commands from LSA and convert into sequence of programs, the beam production machine. Run this programs in parallel generating events datagrams sent to the timing network.
- It's a Etherbone master sending etherbone msg.

CPU - API Bloc
- LSA to Programs
- FPGA - SoftCPU Cluster
- Pairs execution time, events and FECs

FPGA- Event Concentrator
- Aggregates and schedules transmission of events.

Mngmt Master
- It runs network mngt and monitoring software. it configures the network parameters.

Timing Receivers
- Timing Interface of FECs
  Tightly synchronized to the TM Design centered around WB combines the standard func. with specific bus interfaces.

Event-Condition-Action Scheduler Unit
- Generates control signals at pre-programmed times.

White Rabbit SoC
- Generates timestamps triggered by signals

I/O
- Lemo
- LVDS
- HDMI

Etherbone Slave
- Wishbone

Form Factors
- PCIe
- VME
- SCU
- Stand-alone

Integration with GSI Timing
- CRYRING
  20-50 FECs
  90% FAIR features
- Proton Linac Source
  Few FECs + Pulse Generator
  First Production Timing System

Development Plan
- Iteration cycles releasing production Timing Systems

Complexity
- Features
- Scale

Laboratory

2013 2014 2016 2018