SIRIUS CONTROL SYSTEM: CONCEPTUAL DESIGN

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Abstract

Sirius is a new 3 GeV synchrotron light source currently being designed at the Brazilian Synchrotron Light Laboratory (LNLS) in Campinas, Brazil. The Control System will be heavily distributed and digitally connected to all equipments in order to avoid analog signal cables. A three-layer control system is being planned. The equipment layer uses RS485 serial networks, running at 10Mbps, with a very light proprietary protocol, in order to achieve good performance. The middle layer, interconnecting these serial networks, is based on Single Board Computers, PCs and commercial switches. Operation layer will be composed of PC's running Control System's client programs. Special topology will be used for Fast Orbit Feedback with one 10Gbps switch between the beam position monitors electronics and a workstation for corrections calculation and orbit correctors. At the moment, EPICS is the best candidate to manage the Control System.

INTRODUCTION

The Sirius Control System will try to avoid the most commonly found problems in our previous accelerator, the UVX. The lessons learned and the evolution of Control Systems, including in this Information Technology, electronics, software and connectivity equipment, give us the opportunity to design a modern system, heavily distributed, compatible with commercial equipment and customized with proprietary solutions only in restricted areas where high performance is necessary. Long analog signal cables will not be employed anymore due to the short distance between controllers and equipment. When possible the controllers will be inside equipment. For the same reason, crates will be used only where strictly necessary. The three layers adopted, operation, middle and equipment layer, make the system naturally compatible with IP protocol, making the use and configuration of commercial connectivity equipment, such as switches and PC's easier. Unfortunately, the heavy protocol over RS485 industrial serial communication restricts the use of commercial equipment. To get around this, we decided to design and contract local companies to build proprietary hardware with a very light communication protocol over RS485. At the moment we are integrating most of the parts of the system, testing all the solutions proposed and the commercial connectivity equipment.

NETWORK TOPOLOGY

The Sirius Control System will be composed of three layers: operation, middle and equipment. The operation layer will be composed of PC's running client programs, database storages, alarm terminals, etc. The network topology adopted for the storage ring middle and equipment layer will have double star extended architecture, with the first star connecting the high priority equipment (HPE) and the other one the low priority equipment (LPE). In the central point of the HPE there is a high performance workstation with four 10Gbps channels fiber optics interfaces. Each one of the channels will connect a quarter of the storage ring (see Fig. 1).

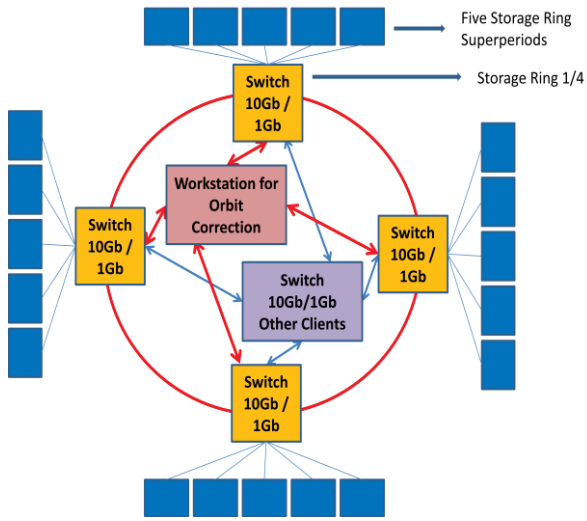

Figure 1: Network Topology.

This workstation, besides the "in hardware" Fast Orbit Feedback under development by the LNLS Diagnostics Group [1], will compute the orbit correction. The correction results will be sent to orbit correctors in the same star way. The LPE star will connect equipment such as power supplies (except correctors), Radio Frequency, vacuum, temperature, etc. In the center of the LPE star there is a switch with four 10Gbps fiber optics interfaces that will distribute data to clients and databases in the operation layer. Alternative fiber optics connections will be implemented, creating a "mesh" and redundant network. In each node of the star extended network there is a switch with 10Gbps interfaces for upload data, over fiber optic, and 1Gbps interfaces for download data, over Cat. 6 cables. Below this level there are only three kinds of equipment: BPM Crates, Single Board Computers (SBC) and switches (see Fig. 2). The BPM Crates are responsible for concentrating the data from BPM and will be better explained in near future[2]. The switches will be used to concentrate other Ethernet equipment. The Single Board Computer will be used as a gateway network to

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encode and decode Ethernet messages to RS485 field bus network, running at 10Mbps. In specific case of orbit correction, this SBC will drive only one or two corrector's power supplies.

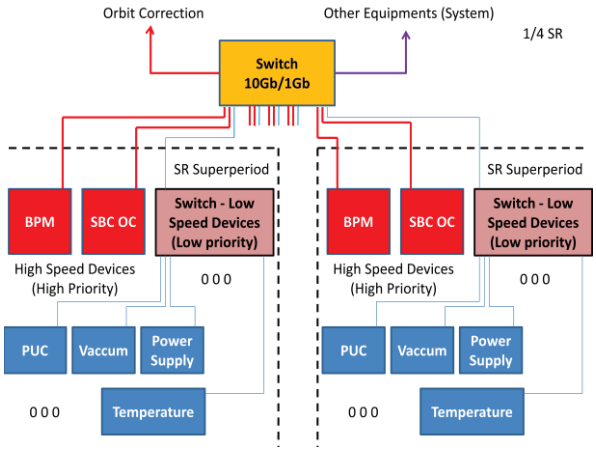

Figure 2: Storage Ring Network Detail.

For this purpose and to achieve good performance, a very light proprietary protocol over RS485 has been written and a fast response time SBC is needed. To test different SBC manufactures, a Linux operational system has been built using the Yocto Project [3], with only basic functionalities, and the time response (RTT – Round Trip Time) was measured over the Ethernet connection using "netperf"[4] from HP Networking Performance Team. Table 1 shows the results obtained.

SWITCHES TESTS

Besides the response time of the Single Board Computers, another critical parameter of the proposed system is the switches latency. Modern switches and routers spend precious time looking for a best way to exchange messages between ports, trying to optimize the network efficiency. In the proposed system this functionality will not be necessary, due the fact that all addresses will be static. Some other features will not be necessary either. In our case, the switches need to receive and retransmit messages as fast as possible. Considering this and using the results of Table 1 for the SBC best, mean and worst result for TCP protocol, another performance test was done to measure the latency of 2 low cost switches, one managed and other unmanaged, both with 8 10/100/1000Mbps ports. The results are presented in Table 2.

Table 1: Round Trip Time for SBC from Different Manufacturers

Processor	Network Interface	Average Time (uS) @100B payload (60 S test)	
		UDP	TCP
(a) AMD Geode LX800 #1core @500MHz - 0.5GB	82551ER @0.1Gbps	148.42	158.84
Intel Core 2 Duo E4600 #2cores @2.4GHz - 4GB Desktop	RTL8169SC @1.0Gbps	58.77	60.45
Intel Core 2 Quad Q8400 #4cores @2.7GHz - 4GB Desktop	RTL8169SC @1.0Gbps	54.24	57.68
Intel Atom 530 #1core @1.6GHz - 1GB	82574IT @1.0Gbps	161.71	161.84
(b) AMD Geode LX800 #1core @500MHz - 0.5GB	RTL8100CL @0.1Gbps	132.98	143.00
Intel Celeron 847 #2cores @1.1GHz - 2GB	RTL8111F @1.0Gbps	227.61	229.12
(c) AMD Geode LX800 #1core @500MHz - 0.5GB	82551ER @0.1Gbps	153.21	164.64
Intel Core 2 Duo SL9400 #2cores @1.9GHz - 2GB	82574IT @1.0Gbps	61.60	80.42
Intel Atom N450 #1core @1.7GHz - 2GB	82567V @1.0Gbps	Boot Problem	Boot Problem
Intel Core 2 Duo SP9300 #2cores @2.3GHz – 4GB	82574IT @1.0Gbps	Boot Problem	Boot Problem

Table 2: Round Trip Time for SBC, Plus Latency Time of Unmanaged and Managed Switches

Processor	Average Time (uS) @100B payload TCP Protocol (60 S test)		
	Direct	Unmanaged	Managed
Intel Core 2 Duo SL9400 #2cores @1.9GHz - 2GB	80.42	101.69	105.41
(b) AMD Geode LX800 #1core @500MHz - 0.5GB	143.00	150.46	158.89
Intel Celeron 847 #2cores @1.1GHz - 2GB	229.12	231.61	245.45

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PERIPHERAL UNIVERSAL CONTROLLER - PUC

In the equipment layer, the network will be based on the RS485 standard, running at up to 10Mbps, and commercial equipment communicating over RS232 protocol. Most of the hardware developed in house will use the RS485 too. The protocol is proprietary and very light, keeping only the necessary information in the headers, working in master-slave environment and synchronizing by token, the token being the master message itself. This protocol is based in the same structure used by UVX, is reliable enough for our applications and is well known by the Control Group. The Control Group proprietary hardware uses a stackable system, with a "main board" based on PIC32 family, running firmware and up to 4 interfaces. The interfaces are of 3 types: general control, digital control and analog inputs. The "general control" has one digital to analog converter with 18 bits resolution in the -10 to +10Vdc range. One analog to digital with the same resolution and range of the DA, sampling at 100 KHz. The "digital control" has up to 24 digital I/O (TTL level), with external isolation when necessary. Finally, the "analog inputs" has four channels with 16 bits resolution in -10 to +10Vdc range, sampling at 10 KHz. The "main board" has additional memory for special events such as "post mortem", with SuperCap backup, for 400 hours (2 weeks) data retention and 32K samplings at 10 KHz (3.2 seconds). The tests have shown good results. The AD converter presents excessive noise, but a new carefully design of the circuit board is under development. Besides the good results using the PIC32 family, another design based on ARM family is in course.

EPICS TRAINING

The best candidate to manage Sirius Control System is EPICS. To learn and test EPICS software, the Control Group has developed an EPICS client and IOCs, running in a shell over the UVX Control System nodes. These IOCs are using a local socket to connect to the UVX control program - Prosac (see Fig. 3). Currently, EPICS is only monitoring the operation of the nodes, without privileges to act over the UVX system. This test gave us the opportunity to learn more about the SBCs, train the operators and, in near future, move smoothly the UVX proprietary Control System to EPICS. The SBCs are running NETBSD[5] in a real control system environment, without failures, since its installation 6 months ago. The EPICS IOC software for Sirius is under development.

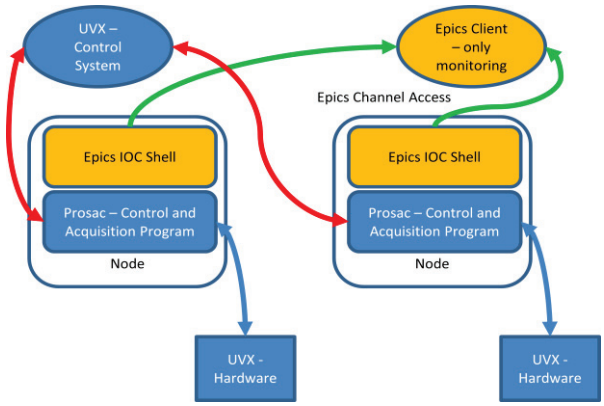

Figure 3: Epics Training in UVX Control System.

CONCLUSION

The proposed system needs more solid and careful tests. At the moment, based on the performed measurements, the possible main point of failure is the latency time of switches and SBC response time. The SBC issue could be solved changing the technology for one more efficient, more powerful and, obviously, more expensive. These SBCs could be used strictly where necessary and another SBC, less expensive, in the other places, to keep the budget within expectation. Besides the good results of the switches tests, we can use the same approach applied to the SBC, and try a new technology too, developed specially for control systems. By the end of 2013, we expect to have a quarter of the Sirius storage ring Control System built in order, to make a more realistic trial.

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