NEW ELECTRONICS DESIGN FOR THE EUROPEAN XFEL RE-ENTRANT CAVITY MONITOR

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Abstract

About one third of the beam position monitors (BPMs) in the European XFEL (E-XFEL) cryomodules will be re-entrant cavities. The BPM mechanics and Radio-Frequency front-end (RFFE) electronics are developed by CEA/Saclay. Two RFFEs and a digital back-end with two ADC mezzanines are integrated into a compact standalone unit called MBU (modular BPM unit) developed by PSI.

The signal processing uses hybrids and a single stage down conversion to generate the signals sum and delta. Every RF/analog component of the re-entrant BPM electronics has been simulated with a Mathcad model and tested independently on test benches. The very low Q of the cavity monopole mode allows the new electronics to filter this mode at the dipole mode frequency, and an I/Q demodulation for delta and sum channels allow the digital back-end to determine the sign of the beam position just by comparing the phases of the channels, independently of beam arrival time jitter and external reference clock phase. This paper describes the design and architecture of a new re-entrant BPM electronics, including results of beam tests at FLASH that were performed to validate the chosen design.

INTRODUCTION

The European XFEL [1] is an X-ray free electron laser user facility currently under construction in Hamburg, Germany. This accelerator has a superconducting 17.5GeV main linac and its parameters are summarized in Tab 1.

Table 1: E-XFEL Accelerator Parameters

Parameter	Value
Normalized projected emittance	1-2 mm mrad
Typical beam sizes (RMS)	20 – 200 µm
Nominal bunch charge	0.1 – 1 nC
Bunch spacing	≥ 222 ns
Macro-pulse length	600 µs
Number of bunches within macro-pulse	1 - 2700
Nominal macro-pulse repetition rate	10 Hz
Maximum macro-pulse repetition rate	25 Hz

The BPM system is developed by a collaboration of CEA/Saclay/Irfu, DESY and PSI. Each cryomodule is equipped with a beam position monitor connected to a quadrupole at the high-energy end of the cavity string. 31 cold BPMs will be re-entrant RF cavities which have to operate in a clean and cryogenic environment. Pickup realisation and mounting in the cryomodule are a CEA/DESY collaboration but are not discussed here [2].

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MODULAR BPM UNIT CONCEPT

The electronics of the European XFEL BPM system [3] follows a modular design approach [4]. This customized crate, called Modular BPM Unit (MBU) (Fig. 1), contains a generic digital back-end (GPAC = generic PSI ADC carrier) with two ADC mezzanine boards, and either four button [3] or two re-entrant or undulator cavity [3] BPM RFFEs, or any combination of those types, as well as power supplies, fans, and a rear IO module with digital and multi-gigabit fiber optic IOs.

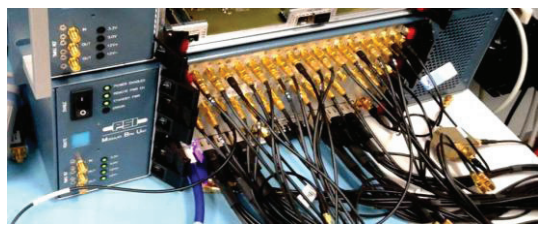

Figure 1: Modular BPM Unit.

RF/ANALOG ELECTRONICS

The signal processing of the re-entrant BPM uses a single stage down conversion to obtain Δ/Σ. The difference Δ and sum Σ signals are obtained from a passive 4- ports 180° hybrid which will be installed in a box mounted at the side of the cryomodule. Each coupler is connected to each pair of opposite antennas and transmits the signals to the radio-frequency front-end (RFFE) electronics via some 30 m long semi-rigid cables. This RFFE electronics, based on a Printed Circuit Board (PCB) with surface mount components, uses the VME64x form factor as required by the Modular BPM Unit. A first electronics was realized in 2010 and tested with beam [2], and a new RFFE with additional functionality is currently being developed.

New Design

The new RFFE analog electronics design, presented Fig. 2, has three channels to perform single-stage downconversion of X position, Y position and reference (charge) RF signals from L-band to an intermediate (IF) frequency. Because of the low external quality factor, the

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single bunch response of the cavity has to be broadened via band-pass filter before its acquisition.

Monopole and dipole mode frequencies of the pickup are respectively 1255 MHz and 1724 MHz [5]. To determine the sign of the beam position, the sum Σ channel of the RFFE will work at the same frequency as the difference Δ channel. The very low external quality factor Q (Q = 24) and the amplitude level of the cavity monopole mode [5] allows the new electronics to filter this mode at the dipole mode frequency 1724 MHz and still obtain a sufficiently large signal level.

On the Δ channel, the rejection of the monopole mode signal, which does not depend on the beam position, is produced by a band-pass filter limited to a 3 dB bandwidth of 110 MHz around the dipole mode frequency 1724 MHz with about 60 dB of attenuation to reject the higher order modes and monopole mode.

Because of the planned operation of the E-XFEL at lower charges from 20 pC to 100 pC, this new design has one input gain range from 0.1 to 1 nC and one from 20 pC to 0.1 nC bunch charge, for the Δ channel. In this second input gain range, the signal is amplified with a low noise amplifier (LNA) and the gain is adjusted thanks to variable attenuators to protect the LNA in different operating modes of the accelerator. The Σ channel has only one gain range and uses the same variable attenuator and LNA. Dynamic range is extended from - 10 dB to 20 dB by switching the gain.

To protect mixers from possible high output power from the antennae, an RF limiter is used on Δ channels. The signal is, then, translated to a lower IF by mixing with a local oscillator (LO) and an in-phase/quadrature-phase (I/Q) demodulation on each channel. The LO drives all three channels with an output power +17 dBm and is locked to the reference signal 216,66 MHz from the linac machine. To generate the LO signal around the dipole mode frequency, a phase-locked loop (PLL) is combined to a divider using an intermediate frequency 9.028 MHz. The I/Q demodulator is composed of mixers used for systems with a high dynamic range, and of 90 ° hybrids couplers chosen for their low phase and amplitude imbalances. This I/Q demodulation for delta and sum channels allow the digital back-end to determine the sign of the beam position just by comparing the phases of the channels, independently of beam arrival time jitter and external reference clock phase. With an 216.66 MHz on-board oscillator integrated to the electronics, the LO can also operate without external reference clock in a free-running mode.

The ADC clock, integrated on the PCB, is also locked to the reference signal and uses a programmable phase shifter and PLL.

Every RF/analog component of the re-entrant BPM electronics has been simulated with a Mathcad model [6] and tested independently on test benches.

The output I/Q IF signals delivered to the ADCs are differential signals. Their shape is close to Gaussian with duration of around 40 ns as shown Fig. 3. The amplitude range is ±1.25V.

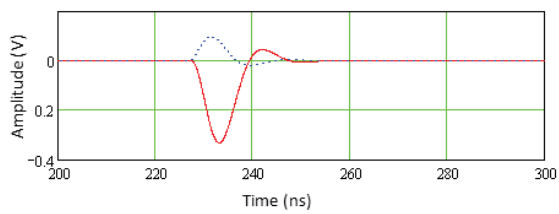

Figure 3: Output I/Q IF signals simulated with a Mathcad model.

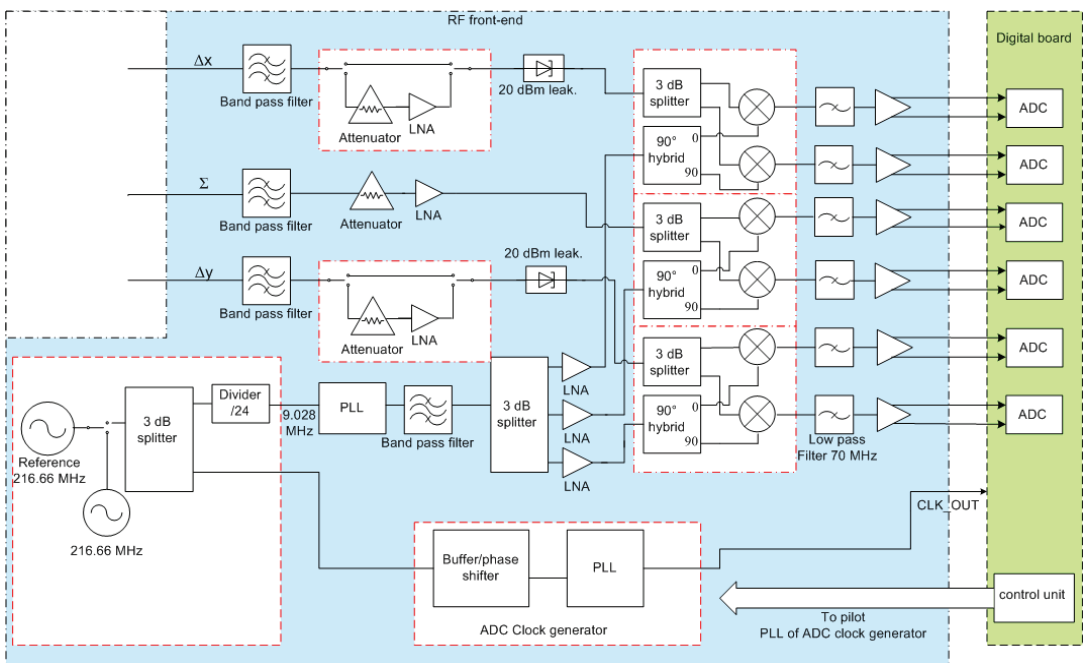

Figure 2: Signal processing electronics.

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Beam Tests

Beam tests at FLASH have been performed in order to validate the new RFFE design for the sum (Σ) signal processing channel.

A simple RF processing electronics composed of a band-pass filter at the dipole mode frequency (1724 MHz), an 90° hybrid and two mixers to do the I/Q demodulation were installed to measure the beam charge. This electronics showed Fig. 4 was connected to cables from the BPM pickup installed in the FLASH linac [5]. A 9.028 MHz machine reference clock signal was used to generate the LO signal for the I/Q demodulation.

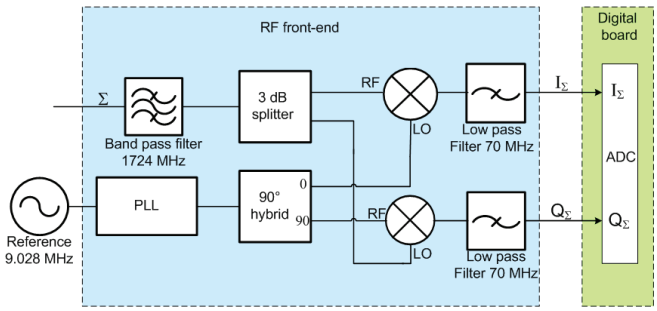

Figure 4: Schematics of the sum (Σ) signal processing.

Signals I_Σ and Q_Σ, generated by the electronics, were connected to the digital electronics composed of fast ADCs with 14 bits resolution [7].

To test the electronics with beam, a re-entrant BPM installed between two toroids, was used to carry out beam tests. The coefficient to determine the charge read by the BPM was obtained from the charge readings of the two toroids. The beam position was moved with steerer magnets in order to see if the Σ channel signal is independent of the beam position. The beam charge was varied via the gun laser energy.

Figure 5 illustrates the charge read by the BPM electronics setup vs charge read by the both toroids. It shows a good linearity of the BPM in a range from 0.1 nC to 1 nC.

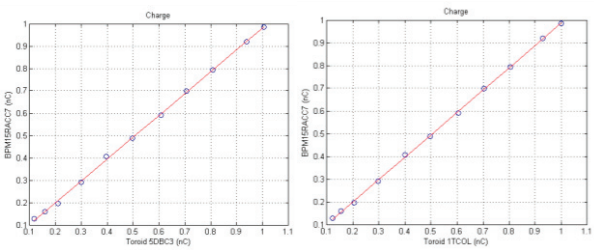

Figure 5: Charge read by reentrant BPM vs charge read by toroids 1TCOLand 5DBC3.

DIGITAL BACKEND

The final version of the re-entrant BPM electronics will use a digital back-end designed by PSI that employs 16 bits ADCs operating at 160 MSPS. The FPGAs on the digital back-end will automatically adjust the ADC clock phase. The re-entrant RFFE output signals for the Σ channel are sampled at its peak and for the Δ channels sampled at their top for a significant offset.

Figure 6: Digital Back-End FPGA Signal Processing Board Prototype [4]. The two large Virtex-5 FPGAs receive the ADC data from the digitizer mezzanines (via adjacent 500-pin connectors, mezzanines removed on photo).

On the present prototype of the digital back-end, two Virtex-5 FPGAs (Fig. 6) on the GPAC calculate beam position and charge from the ADC data, perform automated adjustment of ADC clock phase, RFFE gain and read RFFE status data like temperatures, PLL lock flags, etc... A third Virtex-5 FPGA contains generic firmware/software to control timing and machine interlock system. The electronics supports both an external trigger mode and a self trigger mode where a programmable threshold for the reference channel, i.e. bunch charge, is used as trigger condition.

The MBU has a customized low-cost MBU backplane PCB with direct connections between the different boards plugged into the MBU. However, operation of the boards in normal VME64x crates is also supported, where GPAC and RFFE backplane connectors are interfaced via VME rear transition modules.

SFP multi-gigabit fiber optic transceivers at front and rear side of the MBU, connected to FPGAs on the GPAC, are used for control and timing system interface as well as for exchange of low-latency (microsecond timescale) data with other subsystems like LLRF.

Due to the similar architectures of re-entrant and undulator cavity BPM RFFE, both systems can use the same ADC, digital back-end and nearly identical FPGA firmware. Firmware concept, design and beam tests results are described in detail in ref. [3,8].

CONCLUSION

New electronics design for the re-entrant BPM cavity is being developed in the E-XFEL project. Beam tests were done to check a new design approach for the Σ channel, showing good linearity in a range from 0.1 nC to 1 nC.

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The next step will be the production of the final RFFE board and its test in the MBU, using the GPAC and 16-bit ADCs for digitization and signal processing. Lab tests and beam tests will be carried out to check if the performance meets the E-XFEL requirements.

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